# Thermal Test Die Physical Description

## *General Information*

Diameter: 150mm (6”) nominal

Active Area: Nominal 101 X 101mm (4 X 4”) area in center of wafer

Thickness: 625µm (0.0246" +/-0.001")
(Backside grinding/lapping available as extra cost option)

Backside Finish: Left as processed and typically silicon oxide coated
(Surface smoothness -- can be background and polished as extra cost option)
(Surface metal -- normally not metalized but a variety of metals can be deposited as extra cost option)

Scribe Lane: 76µm (0.003”)

## *Wire-bond Wafer Information*

Topside Passivation: Silicon Nitride ($Si_3N_4$)

Wire-bond Pad: 152µm (0.006”) square

Pad Material: Al-Si(1.0%)-Cu(0.5%)

## *Bumped Wafer Information*

*Note: There is no electrical connection between Unit Cells on the bump wafer version.*

Solder alloy: Pb(95%)-Sn(5%)

UB Material: Al-Si(1.0%)-Cu(0.5%)

UBM Thickness: 10,000Å

Bump height: 100µm

Bump base: 166µm

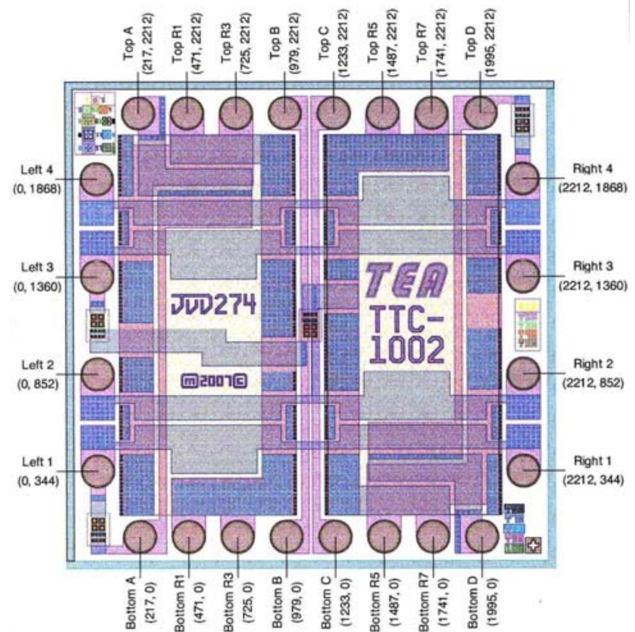
Bump diameter: 169µm

Bump locations: see diagram →

Bump-side Passivation: Polyimide

Stepping Distance = 2540 X 2540 Microns
(Center Scribe to Center Scribe)

Minimum Pad Center to Center = 254 Microns




Disclaimer

Thermal test die are offered for use in characterizing assembly processes, packages, materials and any other applications requiring precise control of heat flux generation and temperature measurement. Applying the data from the test die to a functional system is the responsibility of the user. TEA makes no warranty, express or implied including the implied warranties of merchantability and fitness for a particular purpose, that the user's system designed using that data will perform as intended by the user.

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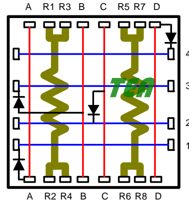
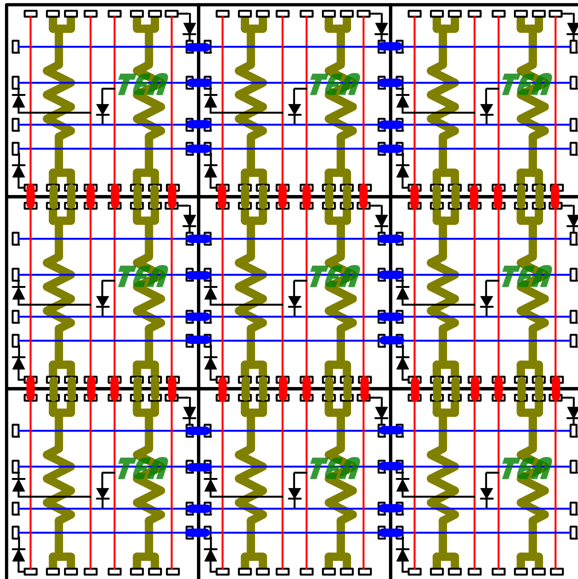



## Unit Cell Representation

## 3X3 Array Respresentation

**(arrays up to 40X40 are possible)**

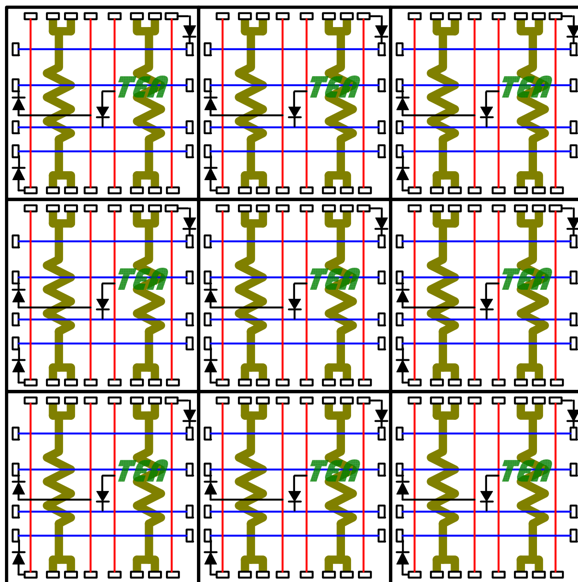


## Wire-Bond Version

Cell-to-Cell Interconnects

- Diode Anode
- Diode Cathode
- Resistor

Only periphery wire bonds required



## Bump (Flip Chip) Version

**NO** Cell-to-Cell Interconnects



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