



Chip Ordering Information

- All thermal test chips are sawn from 625 μ m (0.0246" +/-0.001") thick wafers with the backside left as processed (typically silicon oxide coated). (See Wafer Ordering Information for wire-bond and bump wafer information and for custom backside treatment options.)
- Chips are unbumped and suitable for wire bond applications
(Bumped chips are available on a custom basis – please contact TEA for further information.)
- Pricing on a chip lot basis is as follows:
 - ▶ 1 lot of 20 pcs of unit cell => \$750.00
 - ▶ 1 lot of 10 pcs of 2x2 array => \$750.00
 - ▶ 1 lot of 5 pcs of 3x3 array => \$750.00
 - ▶ 1 lot of 3 pcs of 4x4 array => \$750.00(Other array configurations are available on a custom basis – please contact TEA for further information.)
- Packaging: All chips supplied in a waffle pack.
- All prices are in US\$ and are subject to change without notice.
- Minimum order quantity is one lot; purchase order number and document required.
- Payment Terms are **Net-10 days**
- Shipment
All products will be shipped Ex Works from TEA's facility in California. Freight charges are the responsibility of the purchaser.
- Delivery
In-stock chip lots will be shipped within two (2) weeks ARO
Out-of-stock chip lots will be shipped within thirteen (13) weeks ARO
- Disclaimer
Thermal test die are offered for use in characterizing assembly processes, packages, materials and any other applications requiring precise control of heat flux generation and temperature measurement. Applying the data from the test die to a functional system is the responsibility of the user. TEA makes no warranty, express or implied including the implied warranties of merchantability and fitness for a particular purpose, that the user's system designed using that data will perform as intended by the user.

Note: TTC chips can be optionally supplied in various semiconductor packages – please contact TEA for further information.