Thermal Test Chip Design and Performance Considerations

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Abstract

Increasing device complexity, greater power densities, ever changing packages, and shorter time-to-market deadlines have combined to make thermal characterization efforts more frenzied than ever. A thermal test chip was designed to assist the thermal engineer in answering critical thermal packaging or material questions. It has a standard heat source with integrated temperature sensors in a format that can handle both wire bond and bump chip configurations in a scaleable array size. This allows a single wafer to supply various array sizes to meet changing requirements. The key requirements for a thermal test chip are:

a) Maximum possible heating area relative to chip size.
b) Uniform temperature profile across heating area.
c) Low temperature coefficient for heating source.
d) Temperature sensor in center of chip.
e) Simple-to-use temperature sensor(s).
f) Multiple temperature sensors for a temperature profile across chip surface.
g) Kelvin Connections (i.e., 4-wire connections) for improved measurement accuracy.
h) Chip size that closely approximates the chip being simulated.

This paper will describe a thermal test chip that meets these requirements in the simplest manner possible. Insight into future investigations will also be presented.

Keywords

Thermal Test Chip, Thermal Test Die, Metal Film Resistor, Diode Temperature Sensor

1. Cell Design

The thermal test chip is based on a unit cell that has two resistors and four diode temperature sensors in each cell, as shown in Figure 1. The resistors are deposited metal film resistors that have resistance values suitable for laboratory measurements. Each resistor is 11 Ohms nominal; latter versions will target resistor values of 6 Ohms each to better realize a wide power dissipation range using normally available laboratory power supplies. The two resistors are laid out to occupy 86% of the available area within the electrical contact pads, thus conforming to the JESD51-4[1] 85% coverage requirement; the resistor layout is shown in Figure 2. Note that

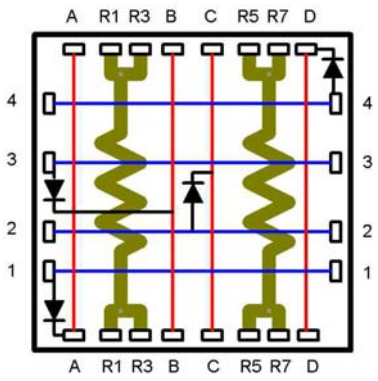

Figure 1. Unit Cell Electrical Layout

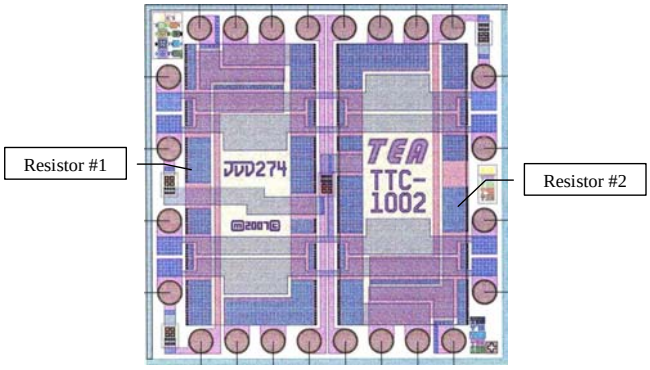

Figure 2 Resistor Coverage

each resistor has two contacts at each end. One contact at each end is used for the power connection while the other contact at each end is used for measurement; this 4-wire Kelvin Connection eliminates contact resistance problems during voltage measurements across the resistor. Compared to polysilicate heating resistors used on other thermal test chips, this metal film version offers better resistance uniformity a (typically ≤±5%) cross the wafer and ≤±2% across a 4X4 array of cells. Figure 3 shows the resistance variation of R_1

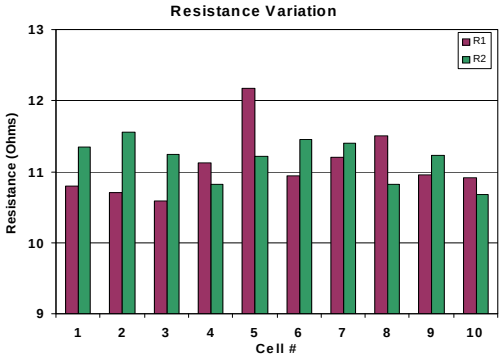

Figure 3 Resistor Variation

and R_2 from a sample of 10 cells across a wafer; the mean resistance values are 11.14 and 11.18 Ohms with standard deviations of 0.38 and 0.30, respectively. The metal film resistors also have low resistance temperature coefficient values, as shown in Figure 4. This attribute results in relatively constant power dissipation over the course of thermal measurements. As a consequence, it enables determining steady state conditions more easily, particularly so during natural convection conditions where it may take up to thousands of

seconds in a natural convection environment. The designed current handing of each resistor, connection trace, and pad is

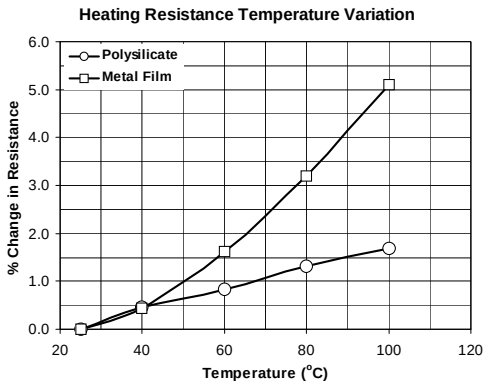

Figure 4 Resistor Temperature Variation

1A, allowing the targeted 11Ω resistor to dissipate up to 11W each.

The four temperature sensing diodes are strategically placed at the center, two diagonals and a center edge, as shown in Figure 5. This serves two purposes. First, these four locations re-present the usual areas of concern when making thermal measurements. Second, these locations are replicated in an array so that there is always a center, two diagonals and a center edge temper- ature sensor in an array no matter how the array is laid out. The characteristics of the diodes are such that a precision 1mA current source will produce a nominal 0.7V across the diode at T_J = 25°C. Each specific diode that will be used for temperature sensing should be subjected to a K Factor calibration for the most accurate junction temperature measurements. However, if the greatest accuracy is not paramount, a sampling of diodes can be calibrated and the

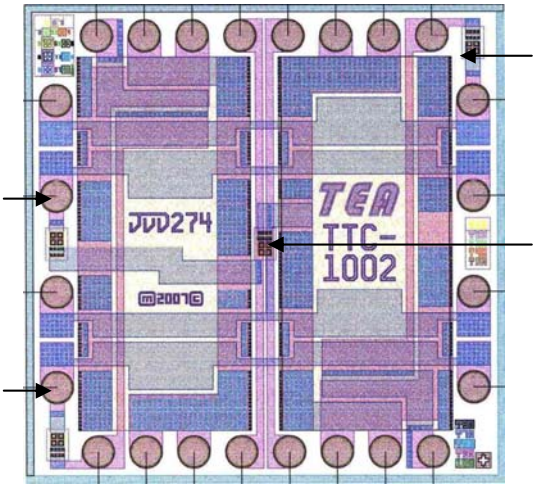

Figure 5. Temperature Sensing Diode Locations

average value used instead of the individual values. Nominal K Factor values are 0.5°C/mV with standard deviations of less than 1%. Each diode is connected to a conductive metal line that runs from one edge of the cell to the opposite edge. This allows Measurement Current (I_M) to be applied to two edges of the cell while Forward Voltage (V_F) measurements are made using separate contacts on the two other edges of the cell.

2. Cell Array

In order for a thermal test chip to be useful in package thermal characterization efforts, the chip size must closely approximate the size of the various application chips that will used that the package. However, given the development and fabrication expenses and the development time, it is not economically feasible to create many specific size thermal test chips. The array approach offers the possibility of combining many unit cells in various manners that better approximate the application chip sizes, see for example [2].

The problem in using arrayed wire-bonded unit cells is that inter-cell wire bonding is necessary to access all the cells. This makes package assembly and use somewhat problematic and relatively expensive. The solution to this problem, if the electrical connection layout allows, is to make the connection metallization in the cell extend beyond the cell boundaries to the next cell. Then when the test chip wafer is cut into the desired array configuration, the inter-cell connections are already in place. The cutting up of the wafer requires a two-pass operation – one pass to remove the metallization in the area to be cut, and a second pass to actually cut the wafer. This two-pass operation will eliminate the resulting problems – metal smearing and metal-to-substrate shorts - that occur with the cutting through aluminum metallization

Figure 6 shows a small 3X3 (≈7.7X7.7mm) array. Note that in this configuration there are six parallel series strings.

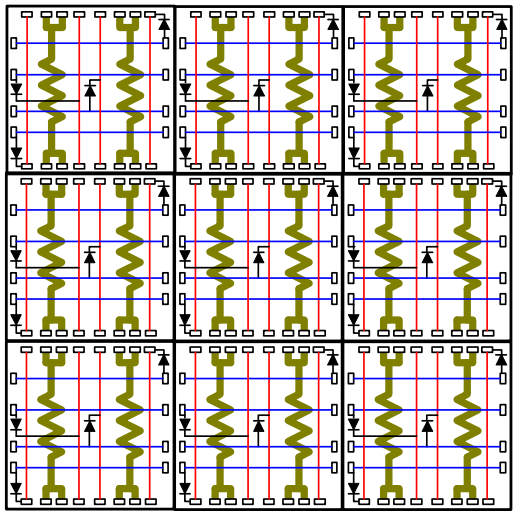

Figure 6. 3X3 Array Layout

Each of these are electrically isolated from the others allowing them to be connected together as a common-power-supply parallel operation or as individually powered series strings. The former is for uniform heating while the latter allows the power applied to each string to be different for power mapping applications. Each series string has a power connection

pad and measurement connection pad on the array periphery, making wire-bonding easy.

The unit cell diode temperature sensor layout results in considerable flexibility in an array configuration. No matter how the unit cells are arrayed, there is always a diode on a diagonal corner, a diode near the center of one side of the array and a diode very near the physical center of the array. These four diodes may connected as 4-wire Kelvin pairs using

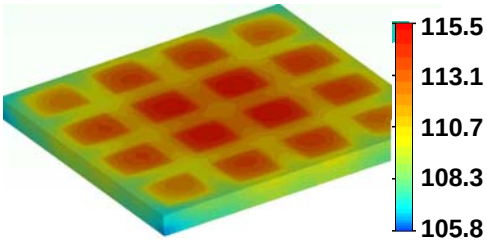

Figure 7. 65% Heating Area Coverage

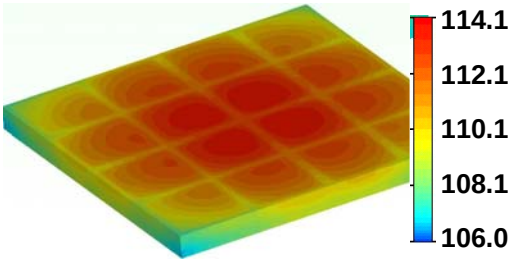

Figure 8. 85% Heating Area Coverage

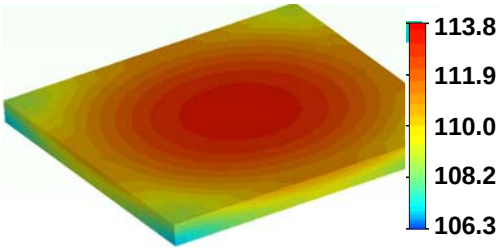

Figure 9. 100% Heating Area Coverage

wire-bond pads on the array periphery. Any of the other array diodes are also available in a similar manner for non-uniform heating applications (i.e., power mapping). It should also be noted that this cell design and wafer fabrication also allows for creation of extreme non-square arrays. For example, a 1X10 array, approximately 2.5 X 28mm, might be used to produce heating loads during thermal tests on linear light source packages. The array can be cut from the wafer in two different ways – either a double string of resistors in series or each resistor isolated. The former has the convenience of minimal power connections if uniform heating is required while the later allows for different power dissipation in each of the 20 heating resistors.

The bumped version of the thermal test chip wafer, in which there is no metallization interconnecting the individual cells, offers even greater flexibility. By using the mounting substrate to implement connection to each unit cells in an array, it is possible to access each heating resistor independently. With connection to the individual temperature sensing diodes in each cell also available at the same time, specific-location temperature measurements can also be made. The total number of heating resistors in any cell is 2N and the corresponding number of temperature sensors is 4N. A 4X4 (≈10X10mm) would have 32 resistors and 64 diodes. Similarly, an array used to simulate a microprocessor-sized chip in the range of 25X30mm, would be a 9X11 configuration with 198 resistors and 392 diodes. The substrate for bumped chip mounting can be designed to provide electrical access to all of these resistors and diodes or, by interconnections between cells, limit the resolution in some areas while maximizing it in other areas. This provides finer grain power application and temperature sensing capability and flexibility to allow for power mapping investigations and for study of spot cooling technologies.

3. Arrayed Test Chip Thermal Simulations

A smaller cell size enables the thermal engineer to more easily customize total die size by dicing the wafer to the desired size using different cell configurations. For example, the 4X4 array test chip considered in the thermal simulations reported below has a unit cell size of 2.5mm x 2.5mm. Hot spots occur naturally, particularly so when the active area is significantly smaller than the total chip area. A keep-out area is required along the edge of the die that cannot include heating elements. The width of the keep-out area is controlled by the width of the saw street (80µm to 100µm), width of crack arresting features (typically less than 5µm) and the size of bonding or bump pads (typically 75µm to 100µm in diameter). Thus, an unheated region extends at least 150µm inward from the edge of the chip. Thermal simulation were conducted using a 35mm body flip chip ball grid array, FCBGA, package and a 10mm x 10mm chip to show the effect of this unheated area. Four different heat area percentages were simulated, 65%, 75%, 85% and 100% based on a 10mm edge-to-edge square die. Three different cooling conditions were considered; no external heat sink (6W), external heat sink (35W) and a cold plate (80W). An isothermal plot for the 35W case with 65%, 85% and 100% heated cell area is shown in Figures 7, 8 and 9, respectively. The temperature drops by approximately 6°C between the unheated regions. A plot of the maximum die temperature as a function of heated area percentage is shown in Figure 10. For the no heat sink case, the junction temperature dependency on source size is hardly noticeable. Θ_{JA} decreased less than 1% for the no heat sink case as the heated area increased 65% to 100%. The heat sink case showed a slightly stronger affect with heated area. Θ_{JA} de-creased by less than 4%. For the cold plate case, a much stronger temperature dependency on heater area was predicted due the higher power levels used for the cold plate simulations. This affect becomes even more pronounced when Θ_{JC} is calculated instead of Θ_{JA}. Since the reference temperature (i.e. case temperature) is closer in absolute value to the junction temperature, Θ_{JC} will be more sensitive to changes in junction temperature. Θ_{JC} increased by 50% while Θ_{JA} increased by 11%.

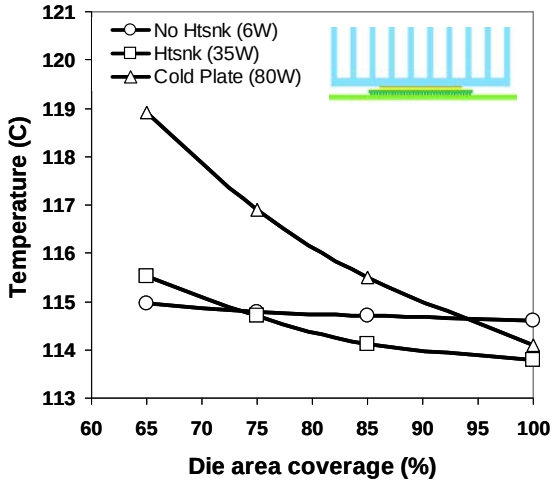

Figure 10. Active die area affect on maximum junction temperature.

4. Future Investigations

Efforts are ongoing to refine and validate the thermal simulations for various different array sizes and configurations and to study the effects of non-uniform heating. Work will also be done to study the long-term reliability of the basic cell and various different arrays so that these test chips can be used in package and system reliability studies as well. Once these efforts are completed. then potential need for larger cell size will also be investigated.

5. Acknowledgements

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[3] Marta Rencz, “The increasing importance of thermal test dies”. Electronics Cooling, September 2000, Vol.6, No.3.