



THERMAL TEST CHIPS

TTC-1002

(2.5mm X 2.5mm Unit Cell)

Wire Bond or Flip Chip

DESCRIPTION

The TTC-1002 thermal test chip is designed to provide a maximum of flexibility for thermal characterization of semiconductor packages. Each unit cell can be used individually or in a square or rectangular array. Strategically placed diode temperature sensors enable temperature measurements to be made in the center, corner and mid-side of an individual die or any configuration array. All diodes, whether in a single die or arrayed die configuration, can be individually addressed, allowing for temperature contour measurements across a unit cell or an array. The two heating resistors on each die can be powered individually or wired in a series or parallel configuration for operation from a single power supply. In an array configuration, there are several resistor series strings that can be individually powered from separate power supplies or paralleled for operation from a single supply. The multiple resistor design allows for thermal measurements with non-uniform heating across the die or array.

FEATURES

- Proven silicon technology
- Format: bumped/flip chip or wire bond wafers or arrays of Unit Cells
- Kelvin connections to heating resistors for improved measurement accuracy
- Array form factor: may be arrayed square or rectangular
- Array configurations: may be arrayed in up to 20 x 20 Unit Cells
- Wire bond: on-chip adjacent cell interconnections of resistors and sensors providing for parallel or series or parallel/series resistor connections with peripheral pad wire bonding
- Bumped: all resistors and sensors may be individually connected
- Two resistors and four sensors per Unit Cell; many resistors and sensors in arrays
- Uniform and non-uniform heating and planar temperature contours capable
- Suitable for both steady-state and transient thermal measurements

Contact TEA for:

- ▶ ReDistribution Layer (RDL) options
- ▶ Bump material composition options, including copper pillars
- ▶ Backside metal and thinning/polishing options

SPECIFICATIONS

Electrical - Heating	TTC-1002
# of Resistors	2
Resistance Value	7.6 Ω \pm 10 % (each resistor)
Resistance Variation	\pm 5 % (for die from a specific wafer)
Max Resistor Power	6 W (6V @ 1A) each
Connection	Force & Sense wire bond or bump pads
Resistor Coverage	>85% of die area within wire bond pads

over, please

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Specification subject to change without notice
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SPECIFICATIONS (continued)

Electrical - Sensing	TTC-1002	
# of Diodes	4 (1 center, 2 opposing corners, 1 mid-side)	
Nominal V_F	0.71 V @ $I_F = 1$ mA each diode	
Nominal BV_R	7 V @ $I_R = 10$ μ A each diode	
Addressing	Row and Column wire bond or bump pads	
Physical		
Wafer Size	152 mm (6 inch) Diameter Nominal	
Unit Cell Size	2.54 X 2.54 mm 0.10 X 0.10 inch)	
Die Layout	See Figure 1	
Array Capability	See Figure 3	
Wafer Thickness	625 μ m (0.025 inch) Nominal (thinning optional)	
Scribe Line Width Between Cells	76 μ m	
Wafer Backside Finish	Ground, un-polished (polishing optional)	
Wafer Yield	Greater than 80%	
Approximate Unit Cells/Wafer	>1200	
Wire Bond Pad Size	166 μ m (0.00654 inch) diameter	
Wire Bond Pad Material	Al-Si(1.0%)-Cu(0.5%)	
Bump Materials available	<ul style="list-style-type: none"> • Lead-Free • SAC305 • Low-Lead • High-Lead 	
Bump Size	~169 μ m diameter, ~100 μ m height	

Figure 1 Unit Cell Layout

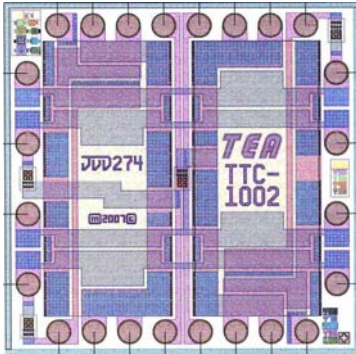


Figure 2 Unit Cell Schematic Representation

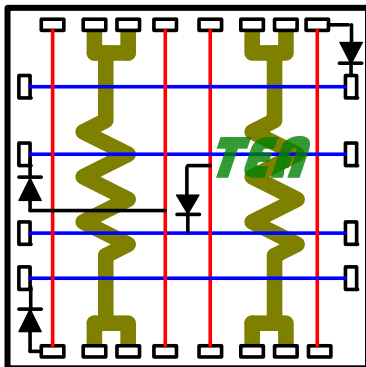
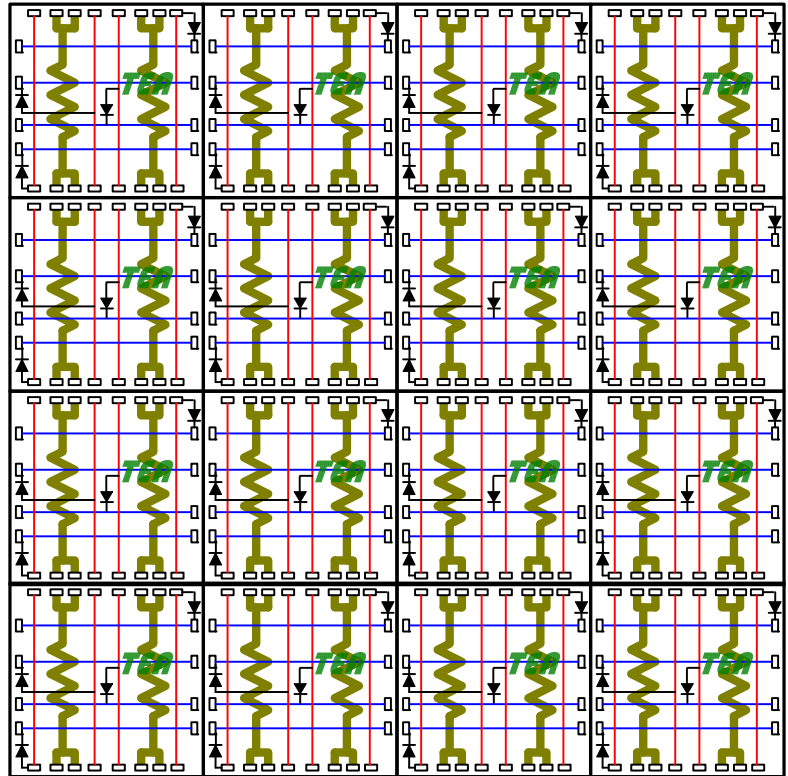


Figure 3 Typical Array Layout (Shown as 4 X 4 array)



For assistance in electrical connection of Unit Cells in an array configuration, please contact TEA with your specific array requirements.